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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,165	12/19/2001	Jose L. Cervantes	10002896-1	6155

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EXAMINER
SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/025,165	CERVANTES, JOSE L.
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/27/04 amendments*.

2a)☒ This action is **FINAL**.　　2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
　　closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 27* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All　b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
　　　　 application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
　　Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-24 and 27 are presented for examination.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claim 27 is rejected under 35 U.S.C. 102(e) as being anticipated by Bui (US Patent No 6,763,478 B1).

4.   As per claim 27, Bui discloses a portable computer having a first battery power mode and a second external power mode, the computer comprising:

a memory bank comprising a plurality of random access memory chips [Fig. 1 and 2; SDRAM memory];

a memory bus in communication with each memory chips [Fig. 1 and 2; col. 5, lines 3-13; memory bus 95];

a control system coupled to the memory bus for reading and writing the memory bank,

the control system including a clock generator, wherein the control system is configured to

operate the memory bank at a first clock speed in the first battery power mode, and a second

clock speed greater than the first clock speed in the second external power mode [col. 5, lines 3-

16, 30-32, 43-51];

a power mode detector configured to provide an indicator to the control system as to

whether the portable computer is in the first battery power mode or the second external power

mode [col. 1, line 62 -- col. 2, line 3; col. 4, lines 26-29];

a keyboard configured to input instructions and data to the control system [Fig. 1 and 2;

I/O controller; col. 1, lines 58-62; col. 2, lines 4-11; col. 4, lines 29-31; col. 6, lines 37-41; by

user command]; and

a drive for storing data, the drive configured to provide data to and receive data from the

control system [inherent to a computer system to have a data drive; col. 1, line 20-24].

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

6.   Claims 1-24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui

(US Patent No 6,763,478 B1) in view of Pecone (US Patent No 5,581,693).

7.   As per claim 1, Bui discloses a portable computer having a first power mode and a

second power mode, comprising:

A first memory bus [Fig. 1 and 2; col. 5, lines 3-13; memory bus 95];

A control system coupled to the first memory bus, wherein the control system is

configured to operate the first memory bus at a first speed in the first power mode, and a second

speed different than the first speed in the second power mode [col. 5, lines 3-16, 30-32, 43-51].

Bui does not expressly disclose about a second memory bus. But a routineer would know

that it is well known in the art to have more than one memory in a system [usually a RAM and a

ROM]. However, Pecone clearly discloses that it is common in a computer system to have more

than one memory bus [Fig. 1; ROM and RAM; col. 3, lines 57-60, 64-65]. Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to have

more than one memory bus in a computer system and thereto controlling the speed of more than

one memory bus accordingly. Moreover, clearly a system will save additional power by

reducing the speed of more than one memory bus and a routineer will do so to extend the battery

life of a portable computer when the portable computer is not operated via an external power

source.

8.	As per claims 11 and 17, Bui discloses a computer having a first battery power mode and

a second external power mode, the computer comprising:

a random access memory [Fig. 1 and 2; SDRAM memory; col. 6, lines 58; RAM

memory];

a first memory bus in communication with the random access memory [Fig. 1 and 2;

memory bus 95];

a control system coupled to the first memory bus for reading and writing the random

access memory, the control system including a clock generator, wherein the control system is

configured to operate the first memory bus at a first clock speed in the first battery power mode,

and a second clock speed greater than the first clock speed in the second power mode [col. 5,

lines 3-16, 30-32, 43-51].

Bui does not expressly disclose about a read only memory and a second memory bus in communication with the read only memory. But a routineer would know that it is well known in the art to have more than one memory in a system [usually a RAM and a ROM]. However, Pecone clearly discloses that it is common in a computer system to have more than one memory bus [Fig. 1; ROM and RAM; col. 3, lines 57-60, 64-65]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have more than one memory bus in a computer system and thereto controlling the speed of more than one memory bus accordingly. Moreover, clearly a system will save additional power by reducing the speed of more than one memory bus and a routineer will do so to extend the battery life of a portable computer when the portable computer is not operated via an external power source.

9.   As per claim 21, Bui discloses a method of managing power in a mobile computing device comprising:

determining whether the mobile computing device is operating in a first power mode or a second power mode [col. 1, line 62 -- col. 2, line 3; col. 4, lines 26-29];

operating a first memory bus at a first bus speed when the mobile computing device is in the first power mode [col. 5, lines 3-16, 30-32, 43-51; operating the memory bus at 66 MHz in the first power mode]; and

operating the first memory bus at a second bus speed different from the first bus speed

when the mobile computing device is in the second power mode [col. 5, lines 3-16, 30-32, 43-51;

operating the memory bus at 100 MHz in the second power mode].

Bui does not expressly disclose about a second memory bus. But a routineer would know

that it is well known in the art to have more than one memory in a system [usually a RAM and a

ROM]. However, Pecone clearly discloses that it is common in a computer system to have more

than one memory bus [Fig. 1; ROM and RAM; col. 3, lines 57-60, 64-65]. Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to have

more than one memory bus in a computer system and thereto controlling the speed of more than

one memory bus accordingly. Moreover, clearly a system will save additional power by

reducing the speed of more than one memory bus and a routineer will do so to extend the battery

life of a portable computer when the portable computer is not operated via an external power

source.

10.   As per claims 2 and 24, Bui teaches that in the first power mode, the portable compute is

operated via a battery power source, and in the second power mode the computer is operated via

an external power source [col. 5, lines 3-16, 30-32, 43-51].

11.   As per claims 3, 4 and 12, Bui teaches that a power mode detector which detects whether

the portable computer is in the first power mode or the second power mode [col. 1, line 62 -- col.

2, line 3; col. 4, lines 26-29].

12.   As per claims 5 and 13, Bui teaches that the second bus speed is double the first bus

speed [col. 5, lines 3-13].

13.   As per claim 6, Bui teaches that a clock generator [Fig. 2; col. 5, lines 3-5; clock

generator].

14.   As per claims 7 and 14, Bui teaches that a bus speed input for switching the portable

computer between the first bus speed and the second bus speed [col. 5, lines 3-16, 30-32, 43-51].

15.   As per claims 8 and 15, Bui teaches that the control system includes processor and a

chipset [Fig. 1 and 2].

16.   As per claims 9 and 16, Bui teaches that the memory bus is in communication with the

chipset [Fig. 1 and 2].

17.   As per claim 10, Bui teaches that an override switch coupled to the control system for

switching the memory bus to the first speed or the second speed [col. 2, lines 4-11; user can

override the default setting].

18.   As per claims 18 and 19, Bui teaches that the mobile computing device is a laptop

computer [col. 1, lines 10-13].

19.   As per claim 22, Bui teaches that controlling a clock generator to determine the memory

bus speed [Fig. 2; col. 5, lines 3-5; clock generator].

20.   As per claim 23, Bui teaches that determining the memory bus speed independent of an

internal processor bus speed [Fig. 2; col. 5, lines 3-51].

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-

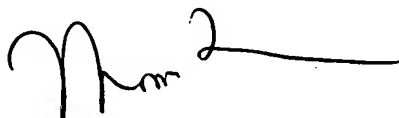3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
February 18, 2005

THOMAS LEE
PATENT EXAMINER
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